IN THE CLAIMS:

1. (previously presented) A system for allowing conventional memory test circuitry to test parallel memory arrays, comprising:

bit pattern distribution circuitry that causes a probe bit pattern generated by said memory test circuitry to be written to each of said memory arrays;

a pseudo-memory, coupled to said bit pattern distribution circuitry, that receives a portion of said probe bit pattern and causes said portion to bypass said memory arrays; and

combinatorial logic, coupled to said pseudo-memory, that employs said bypassed portion and data-out bit patterns read from said memory arrays to generate a response bit pattern that matches said probe bit pattern only if all of said data-out bit patterns match said probe bit pattern.

2. (previously presented) The system as recited in Claim 1 wherein said bit pattern distribution circuitry comprises a multiplexer coupled to said each of said RAM arrays.

3. (previously presented) The system as recited in Claim 1 wherein portion is a single bit.

4. (previously presented) The system as recited in Claim 1 wherein said combinatorial logic comprises comparator circuitry that produces a zero bit only if all of said data-out bit patterns match said probe bit pattern.

5. (previously presented) The system as recited in Claim 4 wherein said combinatorial logic further comprises corrector circuitry that produces said response bit pattern that matches said probe bit pattern only if said comparator circuitry produces said zero bit.

6. (previously presented) The system as recited in Claim 1 wherein said response bit pattern differs from said probe bit pattern by a single bit if at least one of said data-out bit patterns fails to match said probe bit pattern.

7. (previously presented) The system as recited in Claim 1 wherein a portion of said response bit pattern matches a corresponding portion of a data-out bit pattern from one of said memory arrays.

8. (previously presented) A method for allowing conventional memory test circuitry to test parallel memory arrays, comprising:

causing a probe bit pattern generated by said memory test circuitry to be written to each of said memory arrays;

receiving a portion of said probe bit pattern into a pseudo-memory, causing said portion

to bypass said memory arrays; and

employing said bypassed portion and data-out bit patterns read from said memory arrays to generate a response bit pattern that matches said probe bit pattern only if all of said data-out bit patterns match said probe bit pattern.

9. (previously presented) The method as recited in Claim 8 wherein said causing comprises sending a signal to a multiplexer coupled to said each of said RAM arrays.

10. (previously presented) The method as recited in Claim 8 wherein said portion is a single bit.

11. (previously presented) The method as recited in Claim 8 wherein said employing comprises producing a zero bit only if all of said data-out bit patterns match said probe bit pattern.

12. (previously presented) The method as recited in Claim 11 wherein said employing further comprises producing said response bit pattern that matches said probe bit pattern only if said zero bit is produced.

13. (previously presented) The method as recited in Claim 8 wherein said response bit pattern differs from said probe bit pattern by a single bit if at least one of said data-out bit

patterns fails to match said probe bit pattern.

14. (previously presented) The method as recited in Claim 8 wherein a portion of said response bit pattern matches a corresponding portion of a data-out bit pattern from one of said memory arrays.

15. (previously presented) An integrated circuit, comprising:

a processor;

a plurality of identical memory arrays under control of said processor;

conventional built-in test (BIST) circuitry;

multiplexers, associated with said plurality of identical memory arrays and coupled to said processor and said conventional BIST circuitry, that allows said conventional BIST circuitry to take said control from said processor; and

a system that allows said conventional BIST circuitry to test said plurality of identical memory arrays in parallel, including:

bit pattern distribution circuitry that causes a probe bit pattern generated by said conventional BIST circuitry to be written to each of said plurality of memory arrays,

a pseudo-memory, coupled to said probe bit pattern distribution circuitry, that receives a portion of said probe bit pattern, causing said portion to bypass said memory arrays, and

combinatorial logic, coupled to said pseudo-memory, that employs said

bypassed portion and data-out bit patterns read from said plurality of memory arrays to generate a response bit pattern that matches said probe bit pattern only if all of said data-out bit patterns match said probe bit pattern.

16. (previously presented) The integrated circuit as recited in Claim 15 wherein said portion is a single bit.

17. (previously presented) The integrated circuit as recited in Claim 15 wherein said combinatorial logic comprises comparator circuitry that produces a zero bit only if all of said data-out bit patterns match said probe bit pattern.

18. (previously presented) The integrated circuit as recited in Claim 17 wherein said combinatorial logic further comprises corrector circuitry that produces said response bit pattern that matches said probe bit pattern only if said comparator circuitry produces said zero bit.

19. (previously presented) The integrated circuit as recited in Claim 15 wherein said response bit pattern differs from said probe bit pattern by a single bit if at least one of said data-out bit patterns fails to match said probe bit pattern.

20. (previously presented) The integrated circuit as recited in Claim 15 wherein a portion of said response bit pattern matches a corresponding portion of a data-out bit pattern

from one of said memory arrays.